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Final Report

INTERFERENCE APPLIED RESEARCH DATA COLLECTION AND ANALYSIS

Synchronization Of An FIM With A Test Radar

TECHNICAL DOCUMENTARY REPORT NO. RADC-TDR-63-169

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Electromagnetic Vulnerability Laboratory
Rome Air Development Center
Research and Technology Division
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(Prepared under Contract No. AF30(602)-2733 by the Bendix Corporation, Bendix Radio Division, Baltimore 4, Maryland, A.E.F. Grempler, Parker R. Cope, James L. McKain, Walter C. Jackson, Robert E. Barker)

FOREWORD

The feasibility of synchronization of FIM equipment with test radars was first established as a technique by Mr. John Elberson and Lt Dean Baerwald of RADC. The study and investigation described in this report were devoted to further refinement of this technique.

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ABSTRACT

The synchronizing unit to be described substantially reduces the power measurement error inherent in using a field intensity meter to measure a radar set in an area of strong RF interference. With the exception of one electromechanical chopper, the unit is all solid state. The circuits are conservatively designed, although relatively new component types, such as hybrid tunnel diode-transistor logic circuits and field effect transistors, are used to advantage. The significant features of the system are an accurate selection of PRF, automatic gate-width control, timing-error indication and false signal indication. Conventional features such as manual selection of gate-width and automatic correction of PRF are also included in the model. When operated in the automatic gate-width mode, interference signals up to 100 db stronger than the desired signal are effectively suppressed. The performance level of the FIM is maintained, and the receiver is always left in the "on" state if no signal is being received or the SCU is disconnected.

PUBLICATION REVIEW

This report has been reviewed and is approved.

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Subject: EVALUATION OF CONTRACT NO. AF30(602)-2733

1. Synchronization of FIM equipment with test radar has been established as a feasible technique by RADC engineering personnel. This contractual effort has refined the technique and advanced to the point that a production design synchronizing control unit could be established.

2. This effort has provided a system that has the capability of automatic gate-width control, timing-error indication and false signal indication. The synchronizing control unit is capable of reliable operation through its frequency range with no support equipment. With suitable modification kits the unit could be adapted to most field intensity meters.

3. This effort fits into the long-range plan of research and technology in that it provides an interference measurement technique which can be utilized on problems in Electromagnetic Compatibility. Other techniques to be devised from this effort will provide an increased capability in the area of interference measurement techniques in the solution of Air Force problems. In turn, this capability will serve as an input to the DOD Electromagetic Compatibility Program.

Louis F. Moses

LOUIS F. MOSES

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1. INTRODUCTION

This phase of the work performed under contract AF30(602)-2733 for RADC deals with the synchronization of a field intensity meter to a radar set that is under test. A large portion of the ambient environment, which would contribute to false readings on a field-intensity meter (FIM) is eliminated by proper synchronization. This requirement can be accomplished by utilizing the normally fixed pulse repetition frequency (PRF) of a radar transmitter. The feasibility of this technique has been established by Mr. John Elberson, RADC, and is described in a technical paper prepared by Lt Dean Baerwald, RADC. Therefore, the study and investigation was confined to further refinements of this technique. The system used to extend the applicability must contain the following characteristics:

1. Retain the performance level of the basic field intensity meter.
2. Operate without connection to the radar set under test.
3. Maintain the RF integrity of the field-intensity meter and the synchronizer.
4. Use only solid state circuits.
5. Provide a means of automatic gate-width control.
6. Provide a means of recognizing false signals.

The improved technique shall also provide the capability to perform in accordance with the following requirements:

1. Provide selection of PRF between 50 and 2500 pulses per second (pps).
2. Provide a manually adjustable PRF and pulse width.
3. Be capable of synchronizing on the first pulse of the emitter and thereafter automatically correct its own interpulse period to correspond with that of the emitter.
4. Provide for calibration in increments of 0.1 μsec for pulse width and increments of 1 pps for PRF.

2. STUDY PHASE

2.1 GATING

The development of a synchronizing or gating unit for an FIM, to be used when measuring pulse modulated signals, first requires determination of the gating media to be used. The following methods were considered and will subsequently be discussed.

1. Gating between antenna and receiver
2. Gating the first local oscillator
3. Gating the mixer
4. Gating the IF
5. Gating the second L.O.
6. Gating one of the multipliers of the second L.O.

The use of switching ahead of the receiver has the advantage of requiring no FIM modification and thereby is easily adaptable to the different instruments in use; however, available switches leave much to be desired in this type of application. Leakage characteristics result in an on-off ratio which is seldom better than 60 db, and switching time restricts this method to relatively wide gate-widths. The state of the art has not developed to the extent that frequencies above L band can be covered by anything but ferrite devices, which have untolerably slow switching time. The extreme power required and large size of the switches are additional factors which indicate that a different approach to the gating problem is desirable.

Moving into the FIM active circuitry, the first local oscillator was considered for gating. Although very low power is required to turn the first L.O. off, this advantage is offset by the high repeller voltage necessary to accomplish gating. When the klystron L.O. is gated by the repeller voltage, which also determines the operating frequency, the rise and fall time of this gate rapidly sweeps the L.O. through a portion of its frequency range. This condition results in the generation of spurious signals. Also, the impedances involved do not lend themselves to the use of terminated cable. Since the synchronizing control unit (SCU) must maintain the RF integrity of the FIM, this method of gating was abandoned.

Gating the mixer would appear to eliminate the problems encountered with the first L.O. but, as with the switching technique, leakage results in a limited on-off ratio. Even with the mixer inoperative, enough L.O. signal can reach the IF stage, where mixing action occurs, to limit attenuation during the interpulse period.

Similar feed-by problems are encountered when the IF is gated. It is very difficult to obtain adequate decoupling between stages and still maintain a fast rise time characteristic. This limits the on-off ratio to such an extent that multiple stages would have to be gated, and even so, no better than 70 to 80 db could be expected.

The second L.O., being crystal controlled, can not be gated. The narrow bandwidth of the crystal limits the rise and fall times to excessively large values. Under these conditions adequate interference suppression is questionable. The L.O. design could be changed, for example, to an L-C oscillator, to permit gating. However, the unit would have but limited application and would be inherently unstable.

Gating one multiplier of the second L.O. has distinct advantages in regard to impedance matching. Terminated coaxial cable can be used, thereby aiding in maintaining the RF integrity of the FIM and Synchronizing Control Unit. The gating level is also relatively low, which eases this requirement of the control unit, and the multiplier stage can be made broadband to handle the narrow gate requirements. This does bring about a loss in multiplication efficiency due to a reduction in gain, but the problem is easily corrected. The gating efficiency of this method is high, and permits maximum attenuation during the off or interpulse period. All factors considered, this method of gating the FIM seems best suited to the problem and was the basis for the breadboard model.

2.2 SYSTEM LOGIC

With the gating function established, the system logic must be developed. Obtaining the first synchronizing pulse with a gated receiver presents a rather unique problem. If the receiver is off, it can

never receive the first pulse. Therefore, the system must use two receivers, one receiving sync and one video, or it must be assured that when power is applied, the receiver will be on and capable of receiving the first pulse. Furthermore, the trailing edge of the first pulse should initiate a finite off or interpulse period, after which the receiver is turned on until the trailing edge of the next pulse is received. This prohibits the receiver from being locked off by an extra or missing pulse. Another advantage of this system is apparent in the acquisition time. The system requires only that the desired pulse come first, while the repetitive fixed gate method, for example, requires the desired pulse to come at the time of the gate. See Figure 1.

The maximum possible time required for synchronization can be calculated. It is the maximum number of pulses which will probably occur in one interpulse period multiplied by the period of the desired signal. Thus, if but one interference signal of 2500 pps and a 50 pps wanted signal are considered, the maximum is $\frac{2500 \text{ pps}}{50 \text{ pps}} \times \frac{1}{50 \text{ pps}} = 1$ second. If no interference signal is present the unit will synchronize on the first pulse, which results in a maximum time of 1/f.

Although the gate width must be wide enough to bracket the desired signal and tolerate any jitter on the received pulse, it must be recognized that any time between the end of the pulse and the end of the gate is an unnecessary interval during which interference can exist. The interval can be eliminated by causing the trailing edge of the received pulse to terminate the receiver gate. This will provide the unit with automatic control of gate width, and thereby eliminate one control and a source of operator error.

If a condition of zero jitter is assumed, and the synchronization control unit interpulse period is exactly the same as that of the desired signal, the above mentioned method of gate termination will result in equal pulse and gate widths. In such a case the timing of the SCU is exact. If the SCU timing is too fast the receiver gate will open before the pulse arrives and be terminated by the end of the pulse. Thus, a time difference exists between the leading edge of the gate and the leading edge of the pulse. If a voltage or current is generated proportional to this difference, a timing adjustment reference can be made available on a meter.

The foregoing logic can be utilized for automatic correction (AFC) of PRF. However, such a system in the presence of an interference signal with a PRF sub-harmonic within the AFC range of the desired PRF, can be captured with grossly erroneous results and no way of error recognition. This problem is identical to that encountered with automatic range gate tracking in tracking radar sets. Interference signals can also create AFC action causing timing errors and early opening of the gate. Although it is

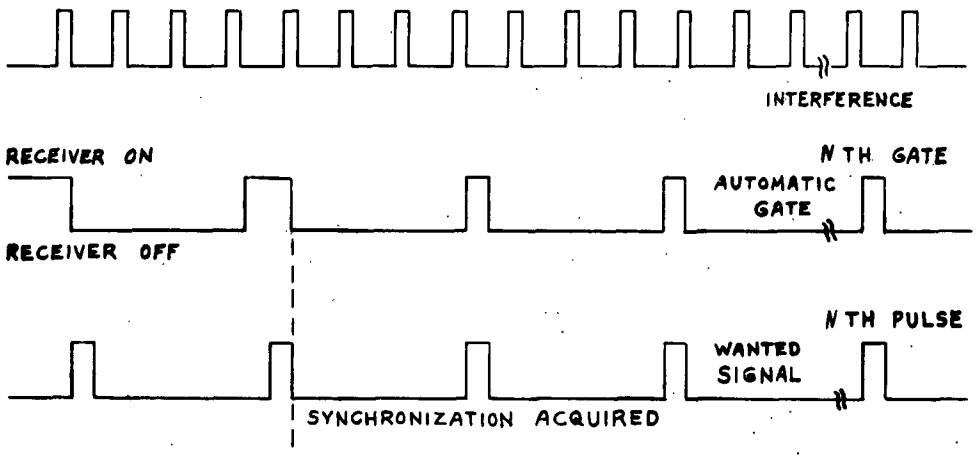


Figure 1. SCU Acquisition Time for Automatic Gating

believed that AFC should be dropped in favor of an accurate and finely timed interpulse period system, it is included in the breadboard model for evaluation purposes.

This will, then, require the timing source to be variable, thereby introducing a device which is in itself unstable. The addition of a chopper-stabilized balancing amplifier can correct this problem, but in turn it limits the amount and rate of AFC correction. However, this is not entirely undesirable since high gain and fast follow rates only add to the capture problem.

The inclusion of a manually controlled gate is necessary for comparison with the automatic gate control. This mode of operation can utilize the interpulse timing circuitry of the automatic gate control, but gate width will be established by a variable delay rather than by the trailing edge of the desired pulse. This mode requires no external synchronizing pulse train for operation. Any starting pulse, such as the transient generated when the unit is energized, will cause it to run free in this mode.

The study phase of this effort indicated that the breadboard model should have the following characteristics.

1. The second L.O. circuit should be gated in a multiplier stage.
2. The gating circuit should function so as to leave the receiver on in the absence of a pulse.
3. The interpulse period should be capable of being calibrated to resolve one PPS at any frequency between 50 pps and 2500 pps.
4. The gate width should be both manually and automatically adjustable to within 0.1 μsec.
5. The model should be well shielded against interference.
6. An error sensor, AFC, should be incorporated.

3. IMPLEMENTATION

3.1 FIM MODIFICATIONS

Two circuits in the FIM were modified by Empire Devices, Inc. to permit optimum synchronization. One of these changes with the appropriate termination networks for the coaxial cable is shown in Figure 2. By utilizing a voltage divider and transistor, a large bias is applied to the cathode of the last doubler of the second L.O. when the synchronizing unit output is sufficiently negative. This negative voltage applied to the base of a 2N708 transistor results in its being turned off. The doubler cathode is then biased beyond cutoff, and no output is obtained from the FIM. When the SCU output is zero or it is not connected to the FIM, the 2N708 conducts and effectively grounds the doubler cathode, which results in normal operation.

The second modification provides a means of maintaining a fixed amplitude sync pulse at any signal level above an MDS, which removes a variable from the design considerations of the SCU. This was accomplished with the tunnel diode transistor thresholding circuit in Figure 3. The output of this circuit is connected to the video output connector of the receiver, so that terminated coaxial cable can be used between the SCU and FIM. The thresholding level is adjusted to permit one error count per second. When the video signal becomes large enough to change the state of the tunnel diode, a video level of 6V appears in the output and remains at this value until the video signal drops below the thresholding level. The SCU sync pulse available from the NF-112 is, therefore, always 6V in amplitude and as wide as the received pulse. This high video level helps override any expected induced signals.

3.2 PASSIVE IMPLEMENTATION

The mechanical implementation of the synchronizing control unit must provide adequate shielding to avoid detrimental effects from radiation or high intensity fields. For this reason, the typical breadboard or temporary setup is inadequate. The entire

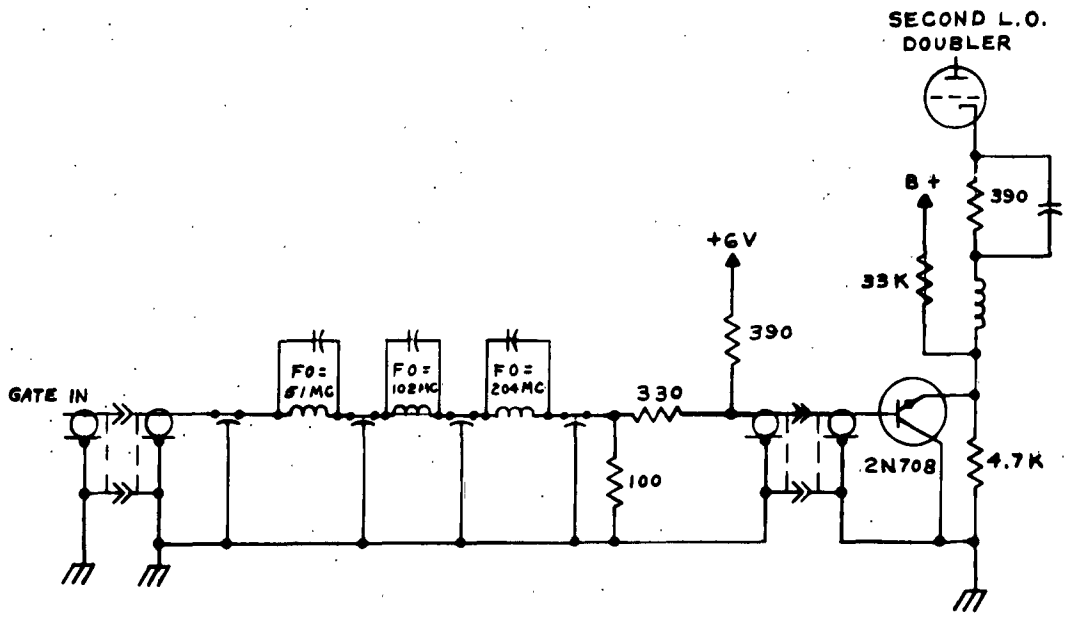


Figure 2. Empire NF-112 Gating Modifications

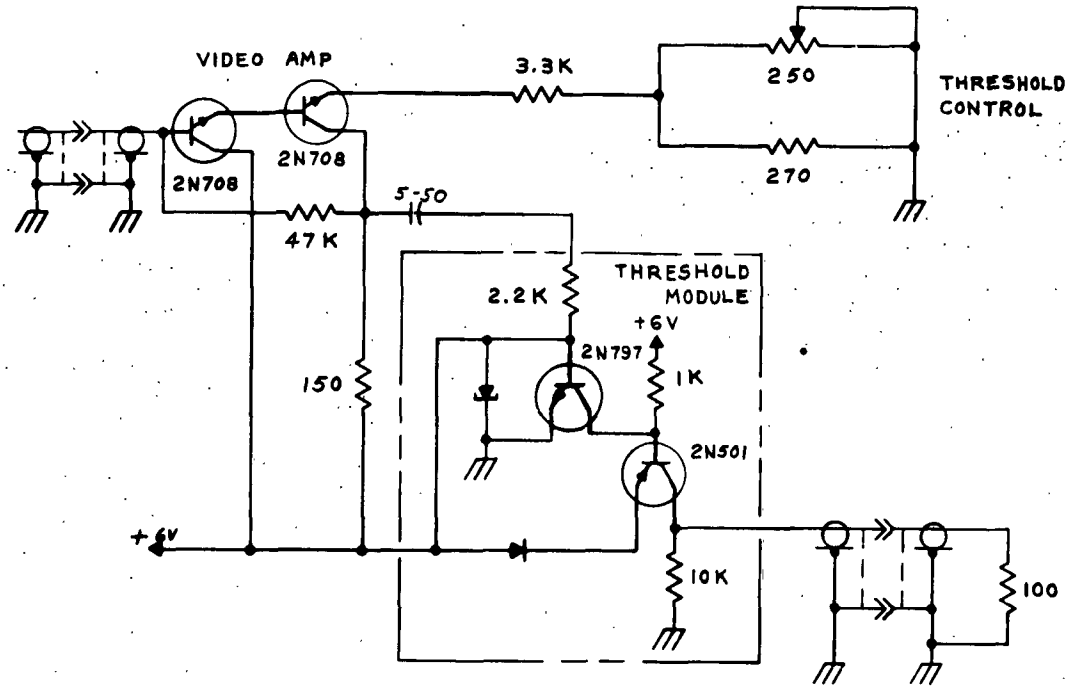


Figure 3. Empire NF-112 Video Output Modifications

circuitry of the SCU was therefore enclosed in a container with brazed seams and the face was then anchored tightly with machine screws around the periphery. The dimensions of the shielded enclosure are 5¼"H x 14½"W x 7¼"D. This shielded compartment was subsequently placed in a dust cover which brings the overall size to 9½"H x 21⅝"W x 14¾"D. A picture of the complete unit is shown in Figure 4.

In the synchronizer, only three unmatched leads enter the shielded compartment: two primary power leads and one meter lead. These are filtered by commercial RF interference filters. Two matched coaxial cables are required to enter the shielded enclosure; a synchronizing pulse and a receiver gate. The control shafts for PRF control, gate-width control and operating mode are coupled through sections of waveguide-beyond-cutoff filters designed for 120 db attenuation at 10 GC. Although quantitative values have not been obtained, these steps to prevent spurious radiation or responses when the SCU and FIM are interconnected are apparently adequate.

3.3 ACTIVE IMPLEMENTATION

3.3.1 Introduction

Converting the positive synchronizing pulse from the modified FIM to a controlled synchronized gate is accomplished within the SCU as blocked out in Figure 5. The waveforms present during the generation of the wanted gate are presented in Figure 6 and permit easy analysis of the gate generation. With the unit in the automatic mode and no synchronizing pulse being received, the voltage states throughout the unit are as at T_0 in Figure 6. Note that under these conditions the receiver is on and ready to receive the first signal pulse. At time T_1 the leading edge of a pulse occurs and initiates the timing circuits. The leading edge of the pulse starts the ramp from the low voltage, or "dumped" level. Thus, the timing is referenced from the leading edge of the first pulse. The trailing edge of the pulse is used to turn the receiver off. The ramp will then rise to a preset level corresponding to the time desired. This is the wanted interpulse period minus 50 μsec. After passing through the 50 μsec delay

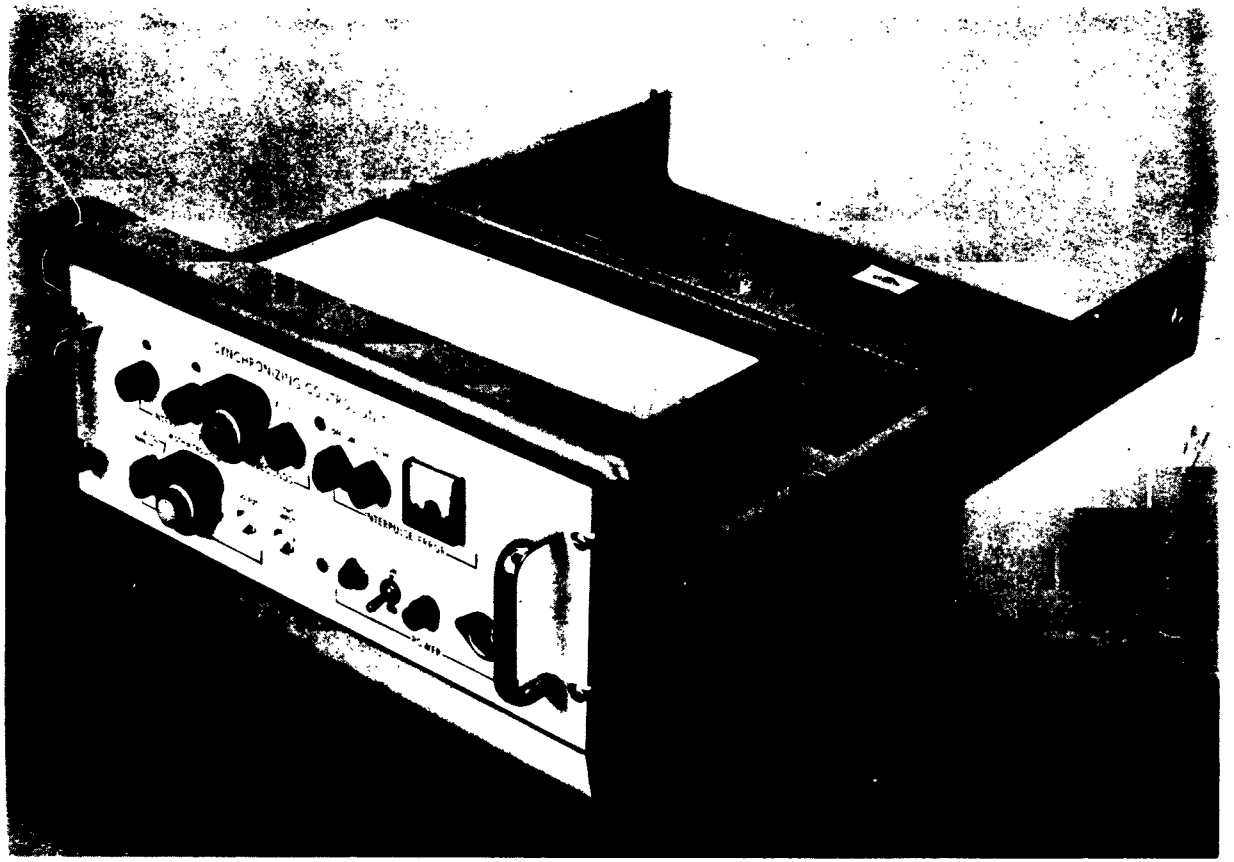


Figure 4. Synchronizing Control Unit

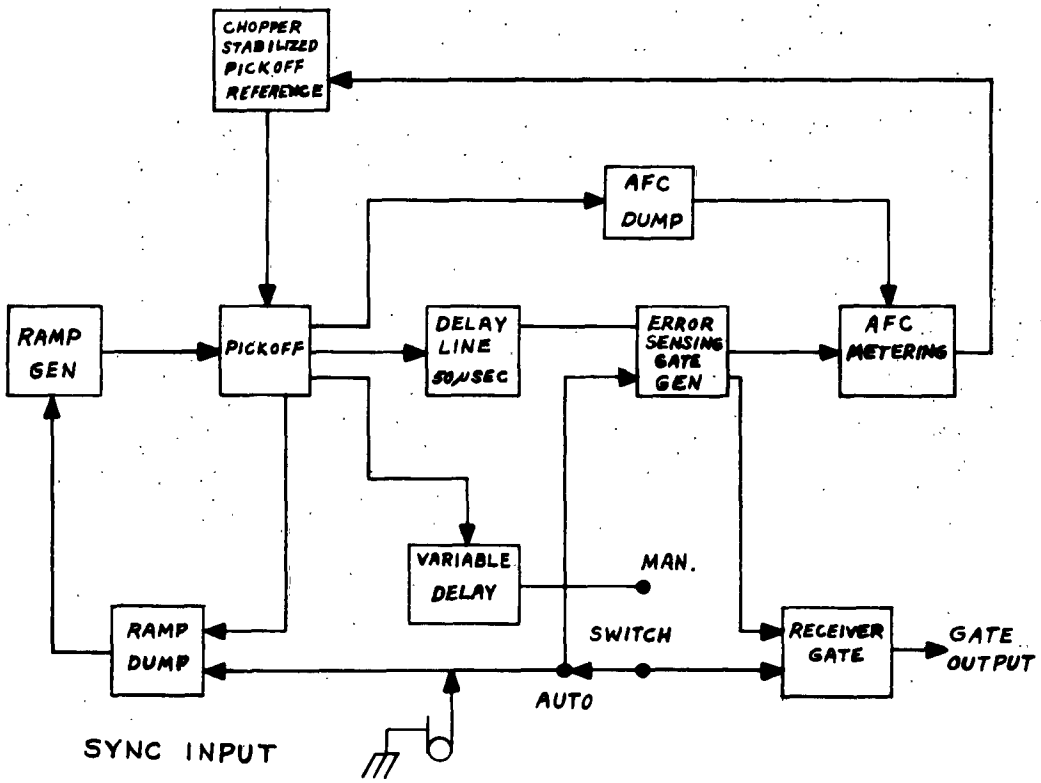


Figure 5. SCU Block Diagram

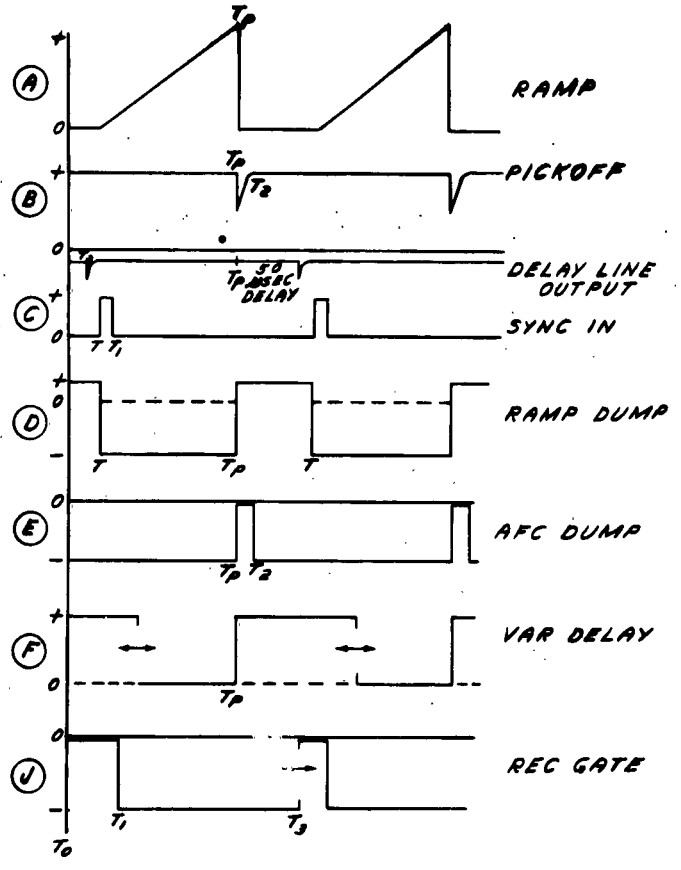
line, the pickoff pulse activates the gating circuit at the desired interpulse time. The receiver has thus been returned to the on state and will remain so until the next pulse triggers the timing cycle. If this signal is a repetitive pulse train, the interpulse period can be adjusted so that the receiver gate opens at the same time the pulse arrives.

The AFC error sensing circuit develops a voltage proportional to the time difference between the leading edge of the gate and the leading edge of the pulse. This voltage is monitored by a meter and is applied, as an error, to a chopper stabilized comparator amplifier. The function of this device is to maintain a constant reference voltage for the pickoff time. An error voltage introduced by the AFC system thus brings about a change in this voltage and the time required for the ramp to reach pickoff. The result is a change in SCU interpulse period, which brings it closer to that of the received pulse.

Operation in the manual mode is identical to operation in the automatic mode except that the gate width is not set by the trailing edge of the wanted pulse, but is timed like the interpulse period. With this basic background, further discussion of the individual circuits making up the SCU follows.

3.3.2 Ramp Generator

A linear ramp generator or timing device for the SCU can be provided by utilizing the charging curve of a condenser when fed from a constant current generator. Figure 7 shows the technique used to provide this type of operation. The Type C632 field effect transistor with a high value of emitter resistance is essentially a constant current device in itself. However, the addition of a chopper stabilized current comparator provides further regulation of current flow in this transistor. The constant current is the charging source for capacitors C_1 and C_2,



T_0 = NO SYNC PULSE (RECIVER ON)
T = LEADING EDGE OF SYNC PULSE (RAMP STARTS)
T_1 = TRAILING EDGE OF SYNC PULSE (CLOSING OF GATE)
T_p = PICKOFF TIME
T_2 = END OF PICKOFF (COMPLETION OF AFC DUMP)
T_3 = PICKOFF PLUS 50 μSEC (GATE OPENS)

Figure 6. SCU Timing Diagram

which are selected and trimmed for a 10:1 ratio. These capacitors in conjunction with the current in the charging circuit, determine the rate of rise of the ramp and thereby the interpulse period. In fact, switching these capacitors provides a 10:1 interpulse scale division, which permits coverage of the specified 50 pps to 2500 pps frequency range.

Since the ramp is the timing device, the performance reliability of the SCU is entirely dependent on the parameters of this circuit. The capacitors must be a precise 10:1 ratio if calibration is to provide convenient scale divisions, and the charging current must be constant if the timing is to be linear. The remaining parameter is the ramp starting level. This

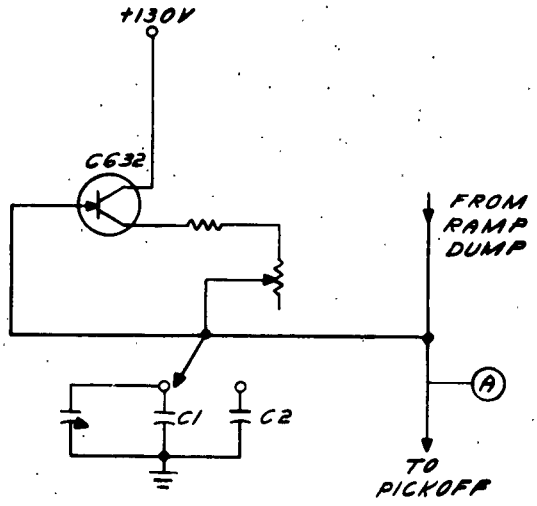


Figure 7. Ramp Generator Circuit

must be constant if interpulse period jitter is to be avoided. As indicated previously, the use of high self-bias on the field effect transistor and a trimmer capacity adequately control the first two parameters, but the only way to insure a constant starting point for the charging curve is to discharge the capacitors prior to the start of the ramp.

3.3.3 Ramp Dump

The ramp dump, which is shown in Figure 8, effectively grounds the timing capacitors prior to the ramp start. If the tunnel diode is negatively pulsed the 2N657 transistor will conduct, permitting discharge of the timing capacitors to the very low saturated emitter collector voltage of the transistor. If the tunnel diode is positively pulsed, it assumes the reverse state, and the current flow in the 2N657 is cut off, which permits the timing capacitors to charge and generate the ramp. It is thus necessary to provide the tunnel diode with a positive pulse at the start of the ramp and a negative pulse at the end of the ramp. The sync pulse from the NF-112, being positive and occurring at the same time the ramp should begin, performs the first task. The negative pulse is obtained from the pickoff circuit which functions as follows.

3.3.4 Pickoff Pulse and Gate Generator

The high input impedance of the field effect transistor is utilized to couple the positive going ramp into the pickoff circuit. (Figure 9.) The output of the field effect is coupled to a unijunction transistor which will fire when the ramp has reached the necessary positive voltage. The output of the unijunction is a positive pulse which is amplified and inverted in a transistor stage. This negative pulse is then fed to the ramp dump as indicated previously. The negative pickoff voltage is also used to trigger the automatic gate leading edge, the AFC dumping transistor and the manual gate timing circuit.

The pickoff time is established by a variable reference voltage applied through a divider to the floating 24V pickoff supply. This reference voltage is varied by step-switching a series of precision resistors, including a ten turn potentiometer with a three digit dial. Five digits are provided by the potentiometer, plus two switches, which permits recording the interpulse period to the required number of places, but the ability to remain in calibration is dependent on the stability of the reference voltage. The fact that AFC is to be incorporated, adds the requirement that the reference be variable and still be ultrastable. A chopper stabilized current comparator was used to accomplish this end.

For the purpose of providing a means of dumping the AFC capacitor, as will be subsequently discussed, the period covered by the ramp is the interpulse period minus 50 μseconds. This 50 μseconds is then added by means of a delay line before gate

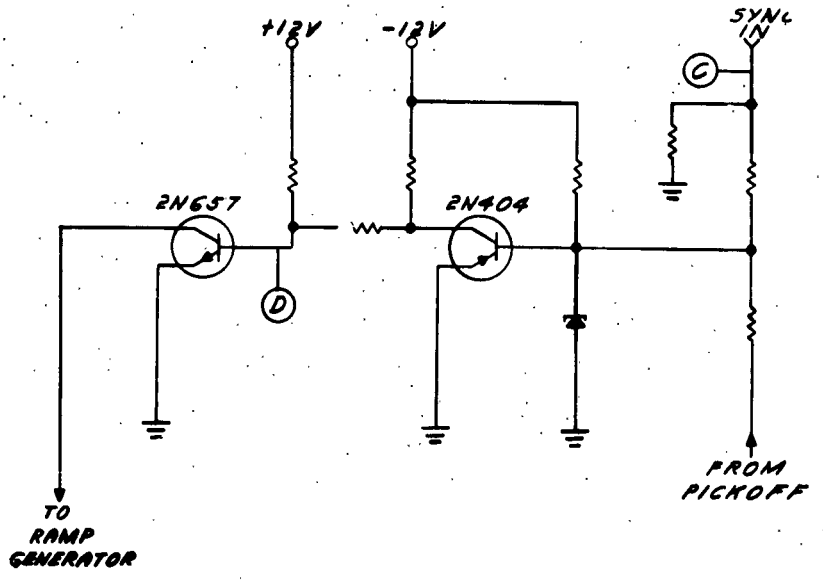


Figure 8. Ramp Dump Circuit

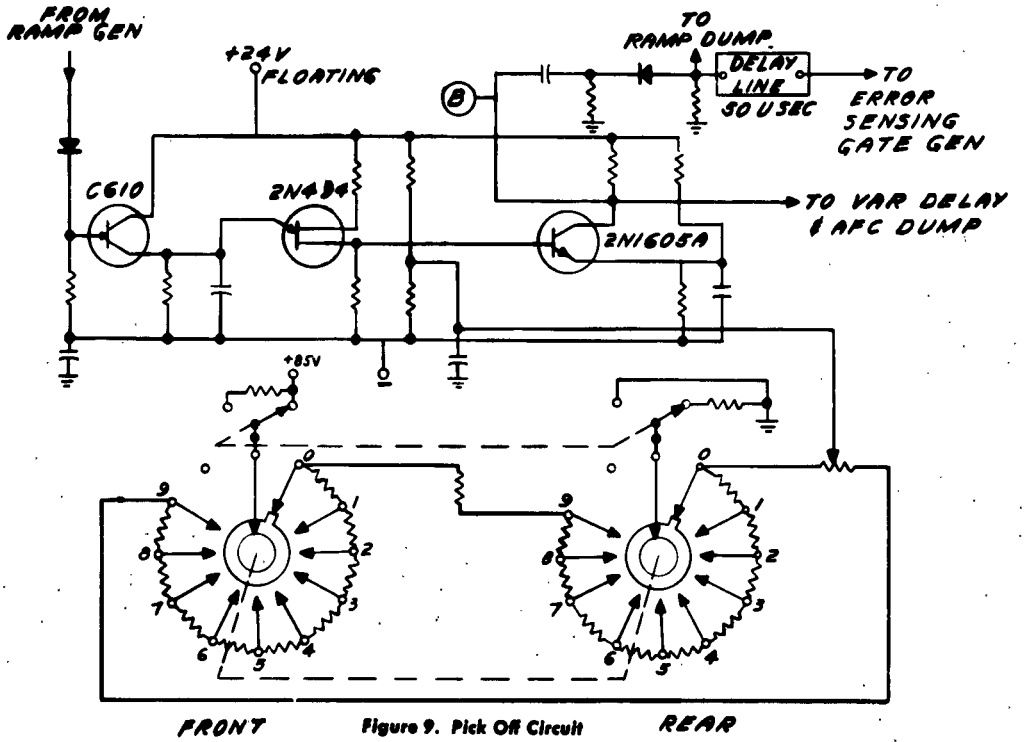


Figure 9. Pick Off Circuit

synchronization takes place. The output of the delay line, which is a negative pulse at the time corresponding to the leading edge of the desired gate, is coupled to a hybrid tunnel diode transistor logic circuit (Figure 10) similar to that used in ramp dump. The tunnel diode reverses state with the negative pickoff which results in a positive going 2N404 collector voltage, which is applied to another tunnel diode-transistor logic circuit (Figure 11). This positive pulse then causes the first transistor in the receiver gate circuit to conduct, thereby applying a positive going pulse to the gate output transistor. The current in the 2N706 transistor is thus cut off and zero output voltage results. Since the output of the SCU is zero, the NF-112 is in the on state and the gate is open. The next received pulse then starts the timing circuits again, but at the same time is differentiated, and the negative portion, corresponding to the trailing edge, is applied to the receiver gate logic circuit. This reverts the tunnel diode to the original state, and the output transistor goes to saturation, resulting in a 10V negative output which is sufficient to gate the NF-112 off.

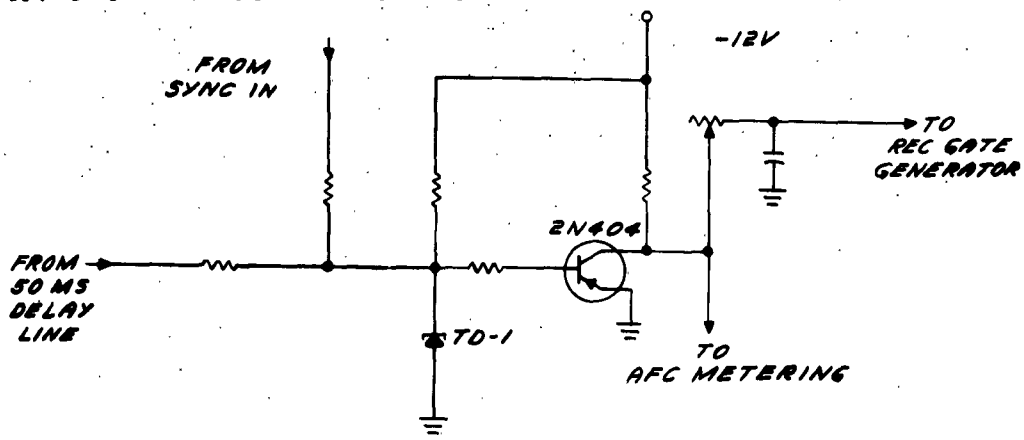


Figure 10. Error Sensing Gate Generator

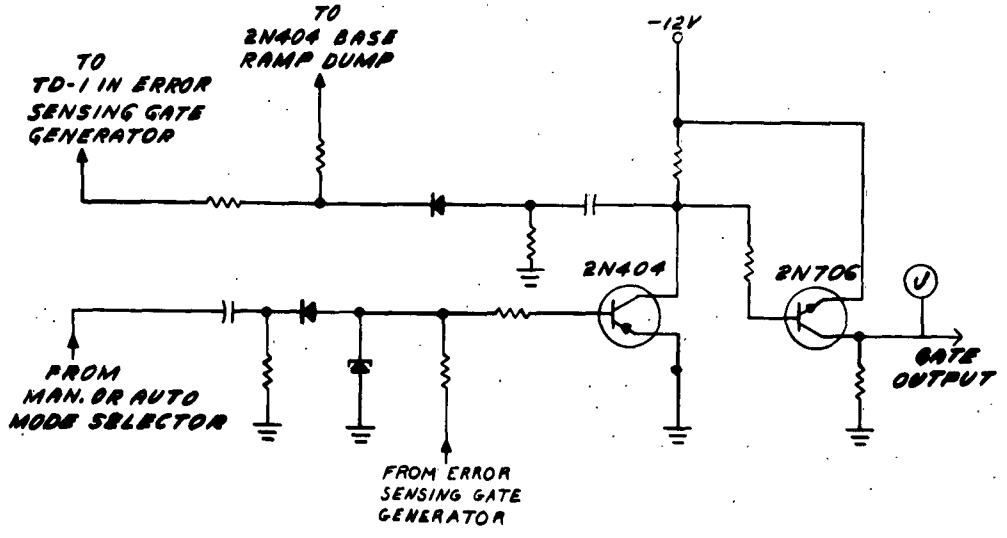


Figure 11. Receiver Gate Generator

3.3.5 Manual Gate

Operation in the manual mode is similar to the automatic with the exception that the NF-112 is not turned off by the trailing edge of the pulse but rather by a variable delay circuit shown in Figure 12. The pickoff pulse causes the 2N1605A to be turned off by reversing the state of the tunnel diode. This applies reverse bias to the 1N116 diode and permits capacitor C_3 to charge from the +85V pickoff reference. By adjusting the series resistance R, the time required for the C610 field effect transistor to conduct sufficiently to turn on the 2N338 transistor can be controlled. When the 2N338 current, which is also controlled by potentiometers R_1 and R_2, reaches a critical level, the tunnel diode will revert to its original state, causing the 2N1605A to conduct again. This will result in a negative going collector voltage, which when applied to the receiver gate logic circuit, will cause the receiver gate to terminate. Also, by using a 10 turn potentiometer with a 3 digit dial in the emitter of the 2N338 (R_2) and properly setting R and R_1, the gate width can be accurately adjusted from 0 to 100 μsec in 0.1 μsec steps. A second 10 turn potentiometer (R in Figure 9) in conjunction with the switching of ten, precision series resistors and the X10 switching of timing capacitors, gives interpulse time adjustment between 400 μsec and 2,000 μsec in steps of 0.1 μsecond and from 2,000 μseconds to 20,000 μseconds in 1 μsecond steps. This provides the capability of easily discerning 1 pps across the design frequency range of 50 to 2500 pps.

To provide an aid to calibration and tuning, the SCU can be made free running when operating in the manual mode. This is accomplished by differentiating the signal at the collector of the 2N404 in the receiver gate and feeding the positive portion back to the ramp dump and gate trigger tunnel diodes. This effectively provides a sync at the time of the gate opening. The sync pulse will trigger the timing circuits and result in the SCU maintaining a repetitive gate. This gate can be counted and used for calibration of the ten turn potentiometer which controls the interpulse period.

3.3.6 AFC System

The AFC error circuitry provides a DC voltage which is proportional to the time difference between the leading edge of the gate and the leading edge

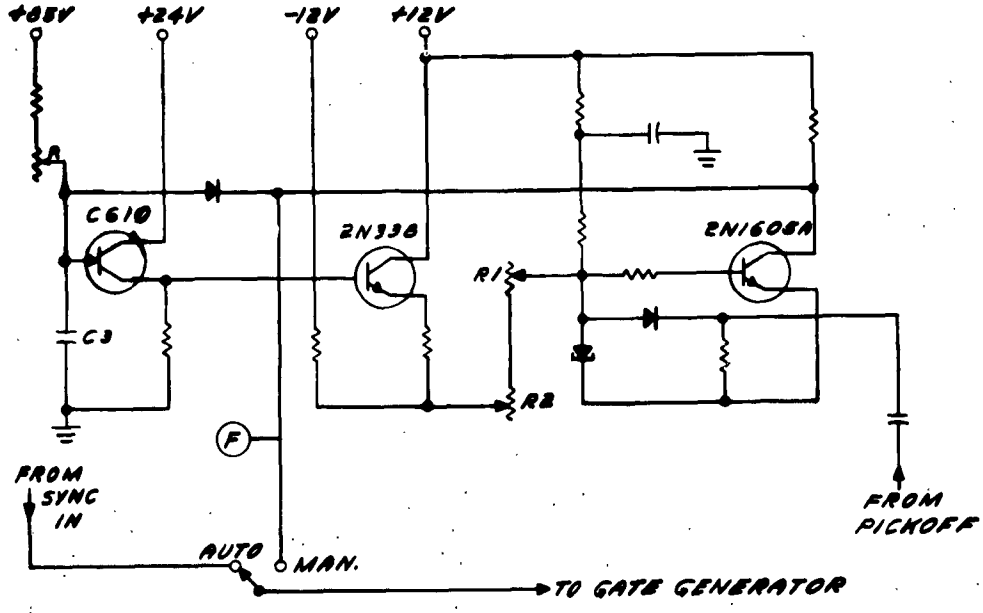


Figure 12. Variable Delay

of the pulse. This is accomplished as shown in Figure 13. With the SCU in the automatic mode and the interpulse period precisely adjusted, the leading edge of the pulse and the leading edge of the gate will be separated in time only by the delay in the gating circuitry, and no error will be introduced. However, if the gate opens before the pulse arrives there will be a switching action by the error sensing gate generator transistor. A positive going pulse will appear at the collector, causing current to flow in the 2N708 during that time. This current charges capacitor C. The resultant output voltage is then fed back to the chopper stabilized current comparator. This AFC voltage acts to adjust the pickoff reference voltage to bring the interpulse period closer to that of the received pulse. The AFC error voltage is also coupled to a metering circuit for use as a fine tuning aid. When the AFC meter is nulled the gate width is approaching optimum.

For the AFC reference to be a function of but one interpulse period, the capacitor C must be discharged between each synchronizing pulse. The dumping pulse can be obtained from pickoff by the addition of the 50 μsec delay as part of the interpulse period. This makes the pickoff pulse occur 50 μsec before the gate and wanted pulse. Thus, the negative pickoff pulse is made to trigger a 2N404 transistor which effectively grounds the AFC capacitor 50 μsec before each gate.

The advantage of an AFC system is in doubt, especially when an accurate and stable interpulse period can be generated. This type of synchronization unit can be captured when the interference signal has a sub-harmonic PRF identical to that of the wanted PRF. If the unit receives the sub-harmonic pulse first, synchronization may be accomplished, and drastically erroneous results will be obtained with no way of detecting the error. If an AFC system is used to correct small changes in PRF, then the sub-harmonic need only be close to the desired PRF to bring about complete capture of the unit.

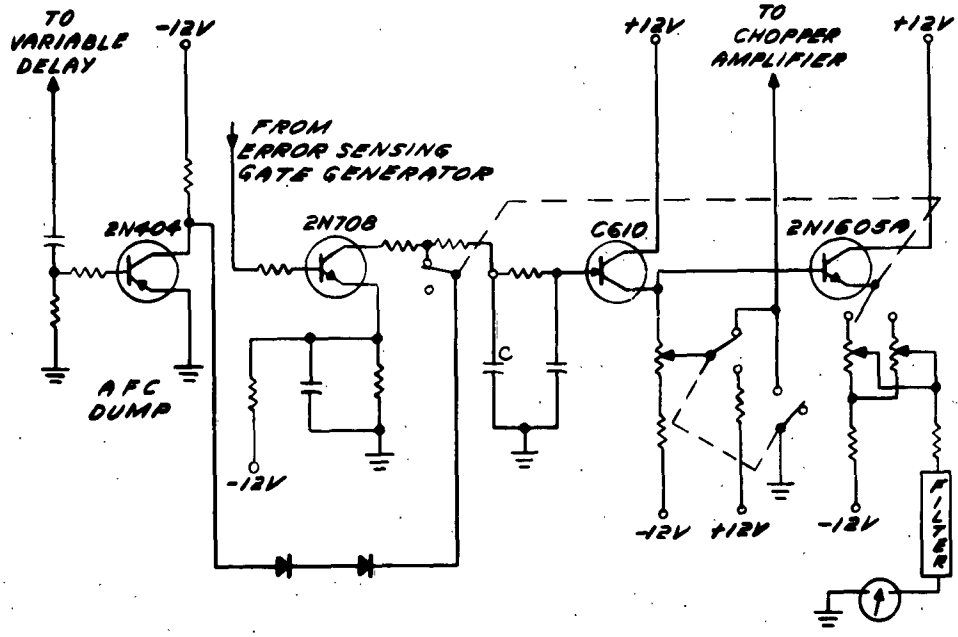


Figure 13. AFC Circuit

4. SYNCHRONIZATION CONTROL UNIT TEST RESULTS

4.1 INTRODUCTION

The test program, utilized for evaluating these improved techniques of gating a field intensity meter in synchronism with a time-limited electromagnetic field, was established to provide interference rejection capability as well as instrumentation techniques. Such operating parameters as AFC and manually adjustable gate width were included. The program required essentially three tests, each being unique in the origin of the electromagnetic field and the number of sources contributing to the field. The environments included those (1) in the Bendix Radio Laboratory at Towson, Maryland, (2) on the Bendix antenna test range, and (3) at RADC's Verona Test Site. The tests conducted in the contractor's laboratory simulate operation in a controlled electromagnetic field, whereas those tests on the Bendix antenna range and the Verona Test Site demonstrate operation in an actual environment and with limited control of the sources of radiation.

An evaluation of techniques is largely subjective since it relates ease of maintaining synchronization, ease of acquiring the desired signal and ease of signal identification. The program accounts for such items by providing tests with and without the synchronizing control unit and with various combinations of control unit functions. Evaluation can thus be made on a relative basis with a minimum of error introduced by auxiliary test equipment.

The present generation of field measuring equipment provides selectivity only in the frequency domain, while the instrumentation improvements to be evaluated provide selectivity in the time domain. Therefore, the effectiveness of the time parameters, inter-pulse period (PRF) and gate width, are of primary concern. These controls were tested in the manual and automatic test modes.

4.2 CONTROLLED ENVIRONMENT IN BENDIX LABORATORY

4.2.1 Measurement of PRF Accuracy

Using a controlled environment in the Bendix laboratory, the synchronizing unit was connected

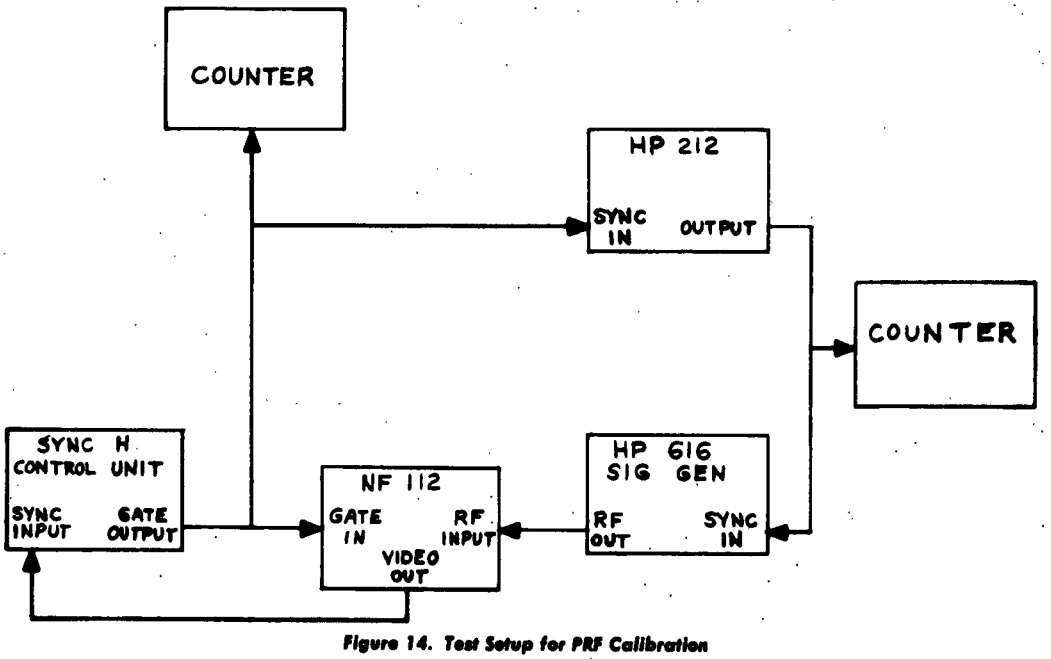


Figure 14. Test Setup for PRF Calibration

with the test equipment as shown in Figure 14 to check the PRF calibration accuracy. The signal generator was set for a nominal RF power, −40 dbm, and a pulse width of 1 to 10 μsec, and the pulse generator was adjusted to the appropriate PRF. External synchronization of the RF generator is required to minimize pulse jitter. With the interpulse error off, the synchronizing control unit interpulse period is set for the value dictated by the generator PRF and the corresponding output PRF recorded from the gate output counter. Typical results obtained from this method are shown in Table 1 and indicate the SCU range to be from 50 to 2500 pps. Similarly, if the SCU is adjusted for identical counter indication and the interpulse is recorded from the SCU djal, an indication of the time domain can be presented. Such data are shown in Table 2 and are indicative of the accuracy to which the interpulse period can be set. It is thus established that the techniques used in the SCU design result in the required range and accuracy.

4.2.2 Automatic Adjustment of PRF

The effect of the AFC system can be determined with the equipment connected as in Figure 15. The signal generator was adjusted to provide a signal PRF 5% below that set on the SCU. The effect of the AFC was to accomplish approximately a 2% correction of the interpulse period. The effectiveness of the system leaves much to be desired as AFC systems go. However, these limitations were accepted since further improvement would considerably multiply the timing stability and capture problems.

TABLE 1

PRF CALIBRATION ACCURACY

Signal PRF (counted)	SCU Interpulse in Seconds	SCU Output (counted)
50	20,000	49
500	2,000	501
1000	1,000	1000
1500	666	1499
2000	500	1999
2500	400	2501

TABLE 2

INTERPULSE CALIBRATION ACCURACY

Signal PRF (counted)	SCU Interpulse in Seconds	SCU Output (counted)
50	19,708	50
500	2,004	500
1000	1,000.4	1000
1500	665.1	1500
2000	500.1	2000
2500	400.2	2500

4.2.3 Measurement of Pulse Width

Evaluation of the pulse width range and accuracy with the unit in the manual mode can be accom-

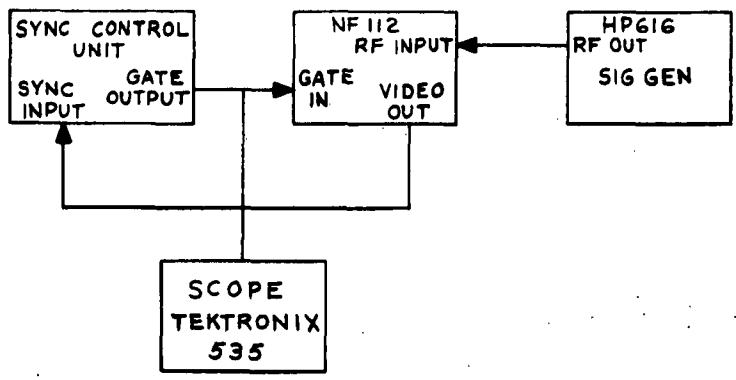


Figure 15. Test Setup for Gate Width Calibration

plished with the test equipment connected as in Figure 15. With the signal generator adjusted to a high PRF (2500 pps) and nominal pulse width and RF power, the manual gate can be set to various points throughout the range, and the gate width measured with a suitable oscilloscope. Data representative of the calibration accuracy is presented as Table 3. It is apparent that the jitter in source PRF and response time of the test equipment result in ambiguous data at exceptionally low gate widths, but it has been established by free running sets that the unit is capable of finer gate widths than are required for adequate interference suppression. This is particularly true when the FIM limitations in regard to pulse widths are considered. Furthermore, the error introduced by improper adjustment of a manual gate appears to make this capability more of a liability than an asset.

The automatic mode results in a gate width which is established by the signal pulse width. The trailing edge of the received pulse terminates the gate and thereby always results in a minimum gate when the unit is properly tuned. The time lapse between the end of a signal pulse and the end of the gate is negligible, and the gate trailing edge precisely follows changes in pulse width.

TABLE 3

CALIBRATION ACCURACY OF MANUAL GATE WIDTH

Gate Width—μsec (dial setting)	Gate Width—μsec (measured)
.1	excessive test equipment jitter
.5	.5 jitter apparent
1.0	1.0
10.0	10.1
50.0	50.2
99.9	100

4.2.4 Suppression of Simulated Interference

Although the foregoing established the fact that the techniques used can be expected to provide synchronization compatible with present radar sets, the primary question as to the ability for interference suppression must also be demonstrated. This was attempted in the laboratory by connecting the equipment as shown in Figure 16. The intentions were to use RF signal generator #1 and the desired signal and #2 as the interference, both tuned to the same RF frequency but with different PRF's. By varying the RF power of the interference signal until an error occurred in the FIM reading the susceptibility could be established for various values of PRF. Attempts to obtain data under these ideal conditions were thwarted by the FIM metering circuit. The decay time of the peak reading voltmeter used in the pulse peak position is in the order of seconds. Thus, very few interference pulses are required to be within the gate in order to maintain an error reading.

A peak pulse metering circuit can be made proportional to the average, median or the mode power. Mathematically, the average value is the sum of the digits divided by the number of digits, and the median is the largest digit plus the smallest divided by two. A large interference pulse can thus result in a gross measurement error if either of these references is used in metering the peak pulse power. However, the mode value, which is the pulse level that occurs most often, is not affected by the few interference pulses which may get through the SCU gate when it is properly tuned. The mode reference can be utilized by incorporating pulse stretching techniques that raise the average power as near to the peak as possible. This permits an averaging meter, with proper calibration, to measure the peak value of the original pulse. Although interference pulses will be stretched and added to the average power measured, the effect can be minimized by insuring the meter will measure each pulse from a common base. The present circuitry does not accomplish this result due to the integration of the interference pulse over many interpulse periods. A meter decay time of several seconds is indicative of this characteristic. Utilization of the pickoff pulse from the SCU to trigger a dumping transistor in the peak reading meter circuitry would alleviate this problem. The pickoff pulse always occurs 50 μsec before the receiver gate, so it is well suited for timing the dumping action. Incorporation of the pulse stretching and dumping techniques in the NF-112 metering circuit would permit direct measurement of the gated peak pulse power.

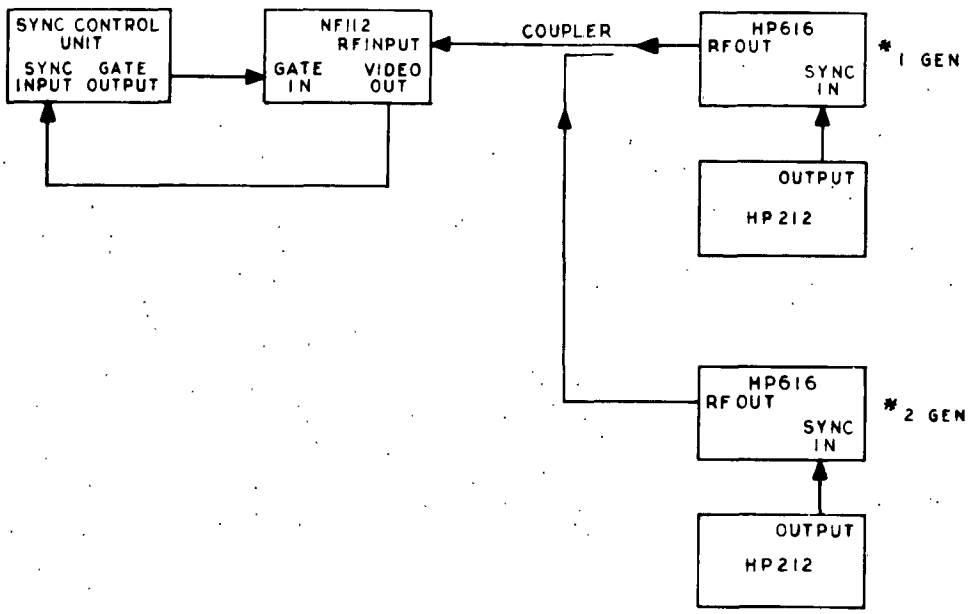


Figure 16. Test Setup for Measuring Suppression of Simulated Interference

Although the above-mentioned modifications were not completed, the NF-112 metering circuit is still to be considered as a function of the FIM synchronizing task. Modification of the metering circuitry was not attempted by the contractor due to its complexity, limitations on funding, and time designated for the completion of this particular effort. For the purpose of these tests the metering problem was circumvented by setting the FIM in the CW peak metering position and using the test set up of Figure 16. Elimination of the peak reading meter from the circuit permitted a reliable evaluation but did not result in pulse peak power readings. Also, very wide pulse widths were required to obtain CW peak power above the noise level and thus give reliable db values. However, the method of evaluation is considered valid and reveals a measurement error of only 1 db when the desired signal in the presence of a 100 db higher interference signal is gated in the automatic mode. Gating in the manual mode results in an error of as much as 15 db, depending on the actual gate width.

Although the foregoing did not result in true peak pulse power of the wanted signal it does show that synchronizing the FIM is practical. Also, metering modifications can be made which will result in normal pulse peak readings from the FIM. This is substantiated by the fact that less than 1 db error in the peak pulse power measurement is obtained when only the desired signal is measured with and without the SCU gating the FIM. The relative signal levels reflected by the 100 db previously stated were also substantiated by measuring the pulse peak powers of the wanted signal and unwanted signal separately and then feeding both signals to the FIM as in Figure 16. The indicator in this case was the audible signal from the FIM video output and/or an oscilloscope on the receiver gate to show any loss of synchronization due to excessive interference. The signal in the phones is an excellent method of determining when interference is being received. False signals can also be identified by monitoring the audible output of the NF-112. When a clean signal is being received, or the synchronizer is operating properly, a single tone at the desired PRF will be heard. However, if synchronization is lost, two tones will be heard, or a coarse tone will intermittently appear. If large unsynchronized interference is being received, a distinctive snap is audible.

4.3 TESTS ON THE BENDIX ANTENNA RANGE

The SCU can be evaluated in an uncontrolled environment by using available radar signals on the Bendix antenna range. To provide control of the power level, PRF and pulse width of one signal, a signal generator was retained in the setup to simulate the desired signal. Figure 17 shows the equipment layout. Without attempting to identify the source, the interference signals were selected by scanning the L-band spectrum with the NF-112 and selecting the interference signals most significant to the test and evaluation of the SCU. The RF generator was tuned to produce a signal at the interference frequency but with a different PRF. The SCU was then set to correspond to the RF generator. The synchronizing and interference suppression capability can be demonstrated using the same techniques employed in the controlled environment. The results of these tests were only pertinent as confirming data since signal levels of the interference were insufficient to result in an observable error. The unwanted signals were adequately suppressed when the desired signal level was above a minimum discernible signal (MDS). A swept PRF radar was used for an interference signal with the wanted PRF inside the sweep range of the interference. The error introduced when the PRF's were coincident did not prevent normal and satisfactory synchronization during the remaining time. Recovery time of the SCU was fast enough to permit accurate measurement of the desired signal at all times except those corresponding to identical PRF's.

The fallacy of a manual gate was again demonstrated by the increased error caused by interference when the receiver gate was progressively widened through its range. The use of an automatic gate width eliminates this source of error.

4.4 TESTS ON THE VERONA TEST SITE

Additional tests were conducted in an uncontrolled environment at the RADC Verona Test Site. The measurement techniques used were similar to those used on the Bendix antenna range. However, the interference signal was much greater in power and higher in frequency (S-band) than the L-band tests made at Bendix. The test equipment setup was identical to that of Figure 17 except for equipment model numbers, which reflect the frequency difference. Synchronizing capability was demonstrated by measuring the interference radar signal with the FIM and then adjusting the RF generator to the same RF but different PRF. The SCU was then set to the PRF of the desired generator signal. With the FIM being gated, the desired signal was attenuated

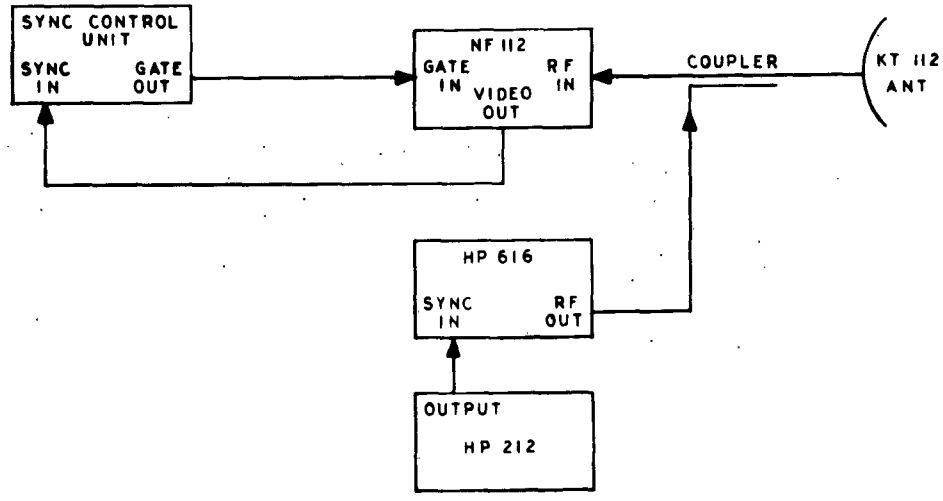


Figure 17. Test Setup for Measuring Suppression of Radiated Interference

until synchronization was lost, as evidenced by the audible tone from the FIM and an oscilloscope monitor on the receiver gate. The signal was then measured with the FIM, and in agreement with the findings at Bendix, the relative levels of desired and interference signals provided a separation of 97 db. Various PRF's were used for the desired signal, including one half the interference PRF and one separated by only 4 pps. The former resulted in typical suppression, but the close separation case gave only a 36 db difference between the interference and desired signals before synchronization was lost. However, 36 db separation between signals so nearly identical considerably advances the present state of the art in field measurement ability. For the Verona tests, the test equipment was located in a van which was driven onto the test range. The interference radar antennas and the FIM antenna were positioned for maximum signal before measurements were conducted. The interfering radar was an MSQ-1 operating at 2,875 mc and with a PRF of 336 pps. Measurements with the NF-112 show a 140 db* power level. The MSQ-1 antenna remained fixed during the duration of the test. Since providing a series of different interference sources did not lend itself to the most expedient test plan, the PRF of the desired signal was varied to simulate a change in radar signals. This provides a reliable test since the RF end of the system has not been altered to incorporate synchronization. Also, the series of evaluations has included operation in both the L and S bands.

The fact that the integrity of the FIM is retained during synchronization was again established by measuring the desired signal with and without the SCU. Less than 1 db of error was introduced.

The ability of the unit to regain synchronization after having lost it through an interrupted signal was demonstrated during the Verona tests. When the desired signal has been attenuated below the MDS level and interference was received, the signal generator output was increased only slightly above the MDS level before synchronization was regained and the 140 db* interference signal suppressed.

*NF-112 Dial reading plus inserted attenuation.

5. CONCLUSIONS

Field intensity meters presently provide selectivity in only the frequency domain, but with proper synchronization considerable selectivity in the time domain can be achieved without impairing the accuracy of the basic unit. The general considerations and methods of implementation which were established by Mr. John Elberson, RADC, and described in a technical paper prepared by Lt Dean Baerwald, have been refined and advanced to the state that a production design SCU could be established.

In reference to the foregoing there are two basic considerations with respect to the electrical performance of the basic receiver: 1. how to accomplish gating and 2. how to obtain the synchronizing pulse. Since the on-off ratio of the receiver limits the degree of interference suppression, the receiver must be gated in a way that provides the greatest attenuation during the interpulse period. Gating the second local oscillator multiplier has proved to be the most effective in the NF-112. The final gating requirements were set so that the receiver was on when the gate voltage was zero. Under this condition the removal of the gate results in normal receiver operation, and performance of the basic field-intensity meter remains unaltered.

Internal generation of an accurate interpulse period permits operation without direct connection to the test radar. This is accomplished by synchronizing a ramp generator with the first pulse of the wanted signal. The sync pulse is obtained from the modified NF-112, which supplies a unit amplitude pulse whenever the instantaneous voltage exceeds the threshold of a tunnel diode circuit installed after the video detector. This provides a fixed amplitude sync pulse at any level above MDS.

Maintaining the RF integrity of the FIM requires the sychronizer to be equally immune to high intensity fields when the units are interconnected. For this reason the typical breadboard is inadequate. This unit has only three unmatched leads entering the shielded compartment. These are filtered by commercial RF interference filters. In addition, two matched coaxial cables enter the shielded enclosure. The necessary control shafts are coupled through sections of waveguide-beyond-cutoff filters designed for 120 db attenuation at 10 GC. These steps to prevent spurious radiation or responses have maintained the RF integrity of the receiver.

To provide a small package with low power requirements the synchronizing unit is all solid state except one electromechanical chopper. The circuits are conservatively designed, although relatively new component types are used. For example, hybrid tunnel diode-transistor logic circuits are used, and field effect transistors are used to advantage where constant current sources and high impedances are required.

The significant features in the system include automatic gate width control, timing error indication, and false signal indication. The automatic gate width control essentially turns the receiver off at the trailing edge of the received pulse, thereby eliminating the need for manual gate adjustment. The advantages of automatic control are apparent when it is recognized that the time between the end of the pulse and the end of the gate is an unnecessary interval during which interference can exist. The error meter provides a visual indication of the time between the leading edge of the gate and the leading edge of the signal. The same logic can be used for automatic correction of PRF. However, in a high interference environment, or in the presence of interference with a PRF subharmonic near the desired PRF, the AFC synchronizer can be more easily captured with grossly erroneous results, which cannot be recognized. False signals can be identified by monitoring the aural output of the NF-112. When a clean signal is being received, or the synchronizer is properly operating, a single tone at the PRF will be heard. However, if sync is lost, two tones will be heard, or a coarse tone will intermittently appear. If large unsynchronized interference is being received, a distinctive snap is heard.

The SCU has two continually variable PRF ranges from 50 pps to 500 pps and from 50 pps to 2500 pps. The readout is capable of resolving at least 1 pps. The manual gate can be resolved to one part in a thousand so the 100 μsec maximum gate width can be adequately calibrated. When properly calibrated and used in conjunction with the modified NF-112, the synchronizing control unit is capable of reliable operation through its frequency range with no support equipment. Further, with suitable modification kits the unit could be adapted to most field intensity meters in use at this time.

6. RECOMMENDATIONS

The techniques utilized in the work covered by this contract can considerably advance the state of the art in regard to field intensity measurement. However, the very narrow pulse width used with some radar sets places an extreme premium on stability of the interpulse period. Therefore, future efforts to provide a production model SCU should include an up to date study of the state of the art to determine the best method of implementing the timing device. Regardless of the method selected for generating an accurate and stable interpulse period, the peak pulse metering circuitry in the NF-112 must be revised to provide a direct indication of the peak pulse power. The ability to make these modifications has been demonstrated on other equipment development projects. If a production design is undertaken, the elimination of the manual gate in favor of the automatic system will insure proper gate width for maximum interference suppression. The use of automatic pulse rate control (AFC) should also be eliminated as evidenced herein. Any refinements should be accomplished within the state of the art of semiconductor devices. A production design could be established from the techniques proposed, and the unit would be practical from the pertinent standpoints of cost, manufacturability and usability. With the inclusion of an appropriate conversion kit, the unit could be designed to accommodate any FIM using heterodyne conversion. The growing importance of reliable field intensity measurements and the ever increasing sources of interference, strongly support a recommendation that these techniques, which represent the most rapid solution to many of the measurement problems associated with pulsed radar sets, be incorporated into a production design.

Rome Air Development Center, Griffiss AF Base, N.Y. Rpt. No. RADC-TDR-63-169. INTERFERENCE APPLIED RESEARCH DATA COLLECTION AND ANALYSIS, SYNCHRONIZATION OF AN FIM WITH A TEST RADAR. Final report, May 63, 28 p., incl. illus., tables.

Unclassified Report

The synchronizing unit to be described substantially reduces the power measurement error inherent in using a field intensity meter to measure a radar set in an area of strong RF interference. The significant features of the system are an accurate selection of PRF, automatic gate-width control, timing-error indication and false signal indication. Conventional features such as manual selection of gate-width and automatic correction of PRF are also included in the model.

1. Synchronization
2. Pulse Discriminator

I. Proj No. 4540, Task 454001

II. Contract AF30(602)-2733

III. Bendix Corp., Baltimore, Md.

IV. A.E.F. Grempler, Parker R. Cope, James L. McKain, Walter C. Jackson, Robert E. Barker

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